very wide data buses, which are entirely different design objectives which result in entirely different architectures.

A key difference between the cache interface architecture design (more specially about the data path design) of the present invention and other prior art designs is that the present invention tries to minimize the number of clock cycles for either read or write operations, including both hit and miss situations. This has not been discussed in any of the prior art.

In order to fulfill this, the present invention has (1) the bi-directional 512 data path at the neck region and a MUX 200, (2) a write buffer 500 directly connected between DQ and Write register 400, (3) a MUX 700 taking inputs either from Read Register 300 or Write register 400 to a read buffer 600 to send them to DQ.

Figure 5 explains clearly how data flow in a write miss case. No prior art data interface will facilitate such a write miss data transfer in a pipe-line fashion.

Write miss is defined as in the cache 100, if we want to write a word line of data in the cache which is 512 wide from external DQ. But somehow we only need to write 1/4 of it, in other words, we must take the other 3/4 from the eDRAM. At this point the 512 bits from eDRAM is loaded to 900 Write Buffer and 64 bit of new data is load to WB 500 and both of them are mapped to Write Register 400, the 64 bits of the new data will overwrite the 64 bits of the old 512 bit data and the whole modified 512 bits data will be send to Cache 100 through MUX 200. At the same time, the old 512 bit data from the Cache 100 are retired from Cache 100 all the way back to eDRAM.

This type of write miss operation is entirely novel relative to the prior art and Leung.

The architecture of the present invention, with the very wide data buses, uses pipe-line operations. Referring to Figure 1 of this application, the very wide bi-directional data bus 1, connecting the SRAM cache 100 through MUX 200 to either read register 300 or write register 400, will not support simultaneous read and write operations.

The described architecture of Leung does support simultaneous read and write operations, and so Leung does not have a similar bi-directional data bus, but must instead use two separate unidirectional data buses.

This patent application has a single independent claim 1, with claims 2-21 being dependent upon independent claim 1. Independent claim 1 specifies in lines 8-9, "a first bi-directional data bus set coupled between the cache memory and both the read register and the write register". This bi-directional data bus is shown as bus 1, which communicates through MUX 200, with either Read Register 300 or Write Register 400, and is a significant component of the present invention for communication between high speed DRAM 1000 and the SRAM cache 200 in the very simple arrangement of Figure 1.

Leung is completely void of a similar bi-directional data bus.

The SRAM cache 187, read buffer 188 and write buffer 189 is described in Leung at C 3, L 12-20, as follows.

"The control circuit includes an SRAM cache, which has the same configuration as each of the memory banks. A cache read buffer is coupled between an output port of the

SRAM cache and the write buffer, thereby facilitating the transfer of data from the SRAM cache to the memory banks. Similarly, a cache write buffer is coupled between an input port of the SRAM cache and the read buffer, thereby facilitating the transfer of data from the memory banks to the SRAM cache."

This arrangement implies two separate uni-directional buses, not one bi-directional data bus.

The arrangement is further described in Leung at the bottom of C 8 and top of C 9 as follows.

Cache read buffer 188 and cache write buffer 189 are coupled to SRAM cache 187. Cache read buffer 188 and cache write buffer 189 enable SRAM cache 187 to perform a read operation and a write operation during the same cycle of the CLK signal. In another embodiment, SRAM cache 187 is fabricated using dual-port SRAM cells, which can be used to support read and write operations during a single cycle of the CLK signal. As described above, SRAM cache 187 is organized as a direct map cache with 256 cache entries, each cache entry containing 256 bits (i.e., eight 32-bit words). Uni-directional internal data bus DA[255:0] couples cache read buffer 188 to write buffer 172. Data bus DA[255:0] carries the data read from cache read buffer 188 to write buffer 172. Uni-directional internal data bus DB[255:0] couples cache write buffer 189 to read buffer 171 (through multiplexer 193). Data bus DB[255:0] carries the read data from read buffer 171 to cache write buffer 189 (through multiplexer 193).

The simultaneous read and write operations described by Leung require two separate data buses, rather than a single very wide bi-directional data bus and MUX (as specified by claim 3).

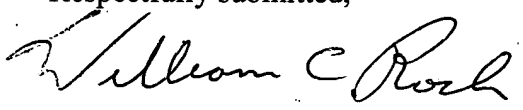
Moreover, the very different design objectives of Leung as described above would not make the single bi-directional data bus arrangement (with the MUX of claim 3) of the present invention at all obvious over Leung.

Additionally, the architecture of Leung will not support the novel write miss operation described above.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with markings to show changes made**".

This application is now believed to be in condition for allowance, a Notice of Allowance is respectfully requested. If the Examiner believes a telephone conference might expedite prosecution of this case, it is respectfully requested that he call applicant's attorney at (516) 742-4343.

Respectfully submitted,



William C. Roch
Registration No. 24,972

Scully, Scott, Murphy & Presser
400 Garden City Plaza
Garden City, New York 11530
(516) 742-4343
WCR/sf
Enclosures Version with markings

"VERSION WITH MARKINGS TO SHOW CHANGES MADE"

IN THE CLAIMS:

Claims 4, 8 and 13 have been amended as follows to obviate the rejections thereof under 35 USC 112.

4. (Amended) The high speed DRAM of claim 1, wherein a sixth data bus couples the read register to a data output from the high speed DRAM ~~circuit~~, and a seventh data bus couples a data input to the high speed DRAM ~~circuit~~ to the write register.

8. (Amended) The high speed DRAM of claim 7, wherein an eleventh data bus couples the DRAM memory to a ~~the~~ write buffer which is coupled through the third data bus to the write register.

13. (Amended) A method of operating the high speed DRAM of claim 3~~1~~, wherein for a read miss operation, a new set of data are retrieved from the DRAM memory to replace old data in the cache memory, and also to be sent to outside data buses through an output read buffer, and during a first cycle of data flow, data flows from the cache memory through the first and fourth buses and is latched into the read register, and data coming from the DRAM memory are latched into the write register through the third bus, and in a second cycle, the directional flows of the data are reversed through the first and fourth buses and also through the third bus.